What is claimed is:

1. A method for fabricating a semiconductor device, comprising the steps of:

forming a plurality of gate line patterns on a substrate with a defined cell region and a peripheral circuit region;

forming sequentially a first insulation layer and a second insulation layer;

forming a first mask layer covering the cell region on the second insulation layer in the cell region and forming a second mask layer in the peripheral circuit region with a predetermined distance from the first mask layer;

etching the second insulation layer with use of the first and the second mask layers as an etch mask to form a spacer at both sidewalls of each gate line pattern in the peripheral region and simultaneously form a guard beneath the second mask layer;

removing the first and the second mask layers;

forming a third mask layer opening the cell region but covering the whole regions including a guard region in the peripheral circuit region; and

performing a wet etching process to the second insulation layer remaining in the cell region by using the third mask layer as an etch mask.

2. The method as recited in claim 1, wherein the second

mask layer is disposed with a separation distance from the first mask layer and opens a boundary region between the cell region and the peripheral circuit region.

3. The method as recited in claim 1, wherein the spacer and the guard beneath the second mask layer are formed through an etch-back process performed to the first and the second insulation layers until a surface of the substrate in the peripheral circuit region is exposed.

4. The method as recited in claim 1, wherein the first insulation layer is a stacked layer of an oxide layer and a nitride layer and the second insulation layer is an oxide layer.

5. The method as recited in claim 1, wherein the step of performing the wet etching process to the second insulation layer is carried out by using hydrofluoric acid (HF).